

REMARKS

Claims 33-60 are pending. Claims 1-8, 14, 16-19, 31, and 32 are rejected. Claims 1-32 are canceled. Claims 33-60 are newly added. No new matter is added.

Examiner Interview Summary

Applicant thanks the Examiner for the teleconference conducted with Nishitkumar V. Patel on November 17, 2010. During the teleconference, the canceled claim 1 was discussed in light of Killian (U.S. Patent No. 5,420,992). The reasons for the lack of teaching or suggestion in Killian are presented below. The Examiner indicated that he will take a close look at the reasons presented below. No agreement was reached.

First Section 103 Rejection

Claims 1-8 are rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Killian et al. (U.S. Patent No. 5,420,992) ("Killian"). Applicant respectfully traverses this rejection.

Claims 1-8 are canceled without prejudice, thereby obviating the rejections. Hence, for at least this reason, Applicant respectfully requests that the Section 103 rejection of claims 1-8 be withdrawn.

Second Section 103 Rejection

Claims 14, 16-19, 31, and 32 are rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Killian in view of Wittig et al., "OneChip: An FPGA Processor with Reconfigurable Logic" ("Wittig"). Claims 14, 16-19, 31, and 32 are canceled without prejudice, thereby obviating the rejections.

New Claims

Claims 33-60 are newly added.

Independent claim 33 recites that “said subcircuitry is operable to use the multi-byte branch instruction to bypass access to a first byte of a multi-byte target instruction to access another byte of the multi-byte target instruction”, as claimed. In contrast, Killian discloses that “the 32-bit instructions actually manipulate 64-bit entities” (column 12, lines 32-37). “A *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention. *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997)” (MPEP §2144.05). Killian teaches away from the feature that recites that “said subcircuitry is operable to use the multi-byte branch instruction to bypass access to a first byte of a multi-byte target instruction to access another byte of the multi-byte target instruction”, as claimed, because Killian discloses that a 32-bit instruction manipulates a 64-bit entity. The 32-bit instruction accesses the entire 64-bit entity. This is contrary to the claimed feature in which “said subcircuitry is operable to use the multi-byte branch instruction to bypass access to a first byte of a multi-byte target instruction to access another byte of the multi-byte target instruction”. Hence, Applicants respectfully submit that claim 33 would not have been obvious over Killian.

For at least reasons similar to those set forth above with respect to claim 33, Killian does not teach or suggest a method as recited in claim 43 or a computer-readable medium as recited in claim 52. Dependent claims would also not have been obvious over Killian at least by virtue of their dependency.

Conclusion

Accordingly, it is believed that this application is now in condition for allowance and an early indication of its allowance is solicited. Should the Examiner believe that a telephone conference would expedite the prosecution of this application; the undersigned can be reached at the telephone number set out below.

Please charge any required fees or credit any over payments to Weaver Austin Villeneuve Sampson LLP deposit account 504480.

Respectfully submitted,
Weaver, Austin, Villeneuve, and Sampson LLP
/James E. Austin/
James E. Austin
Reg. No. 39,489



Nishitkumar V. Patel
Reg. No. 65,546

P.O. Box 70250
Oakland, CA 94612-0250
(510) 663-1100